



Fig. 1

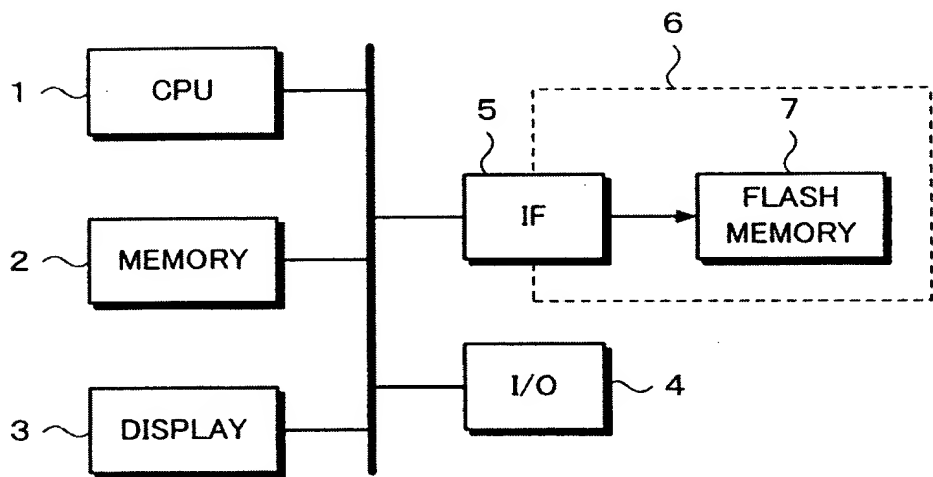


Fig. 2

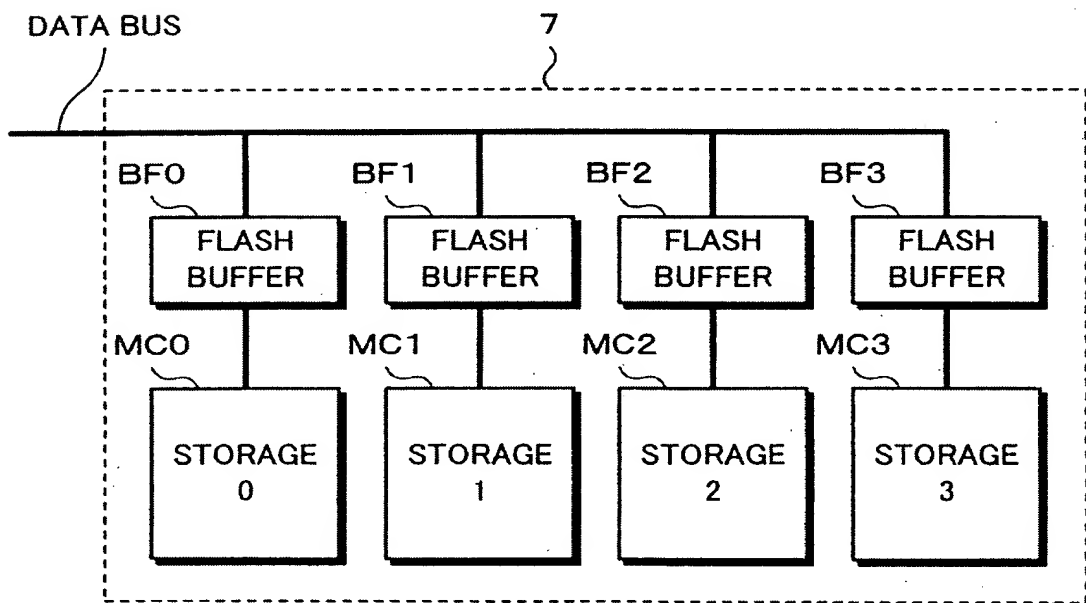
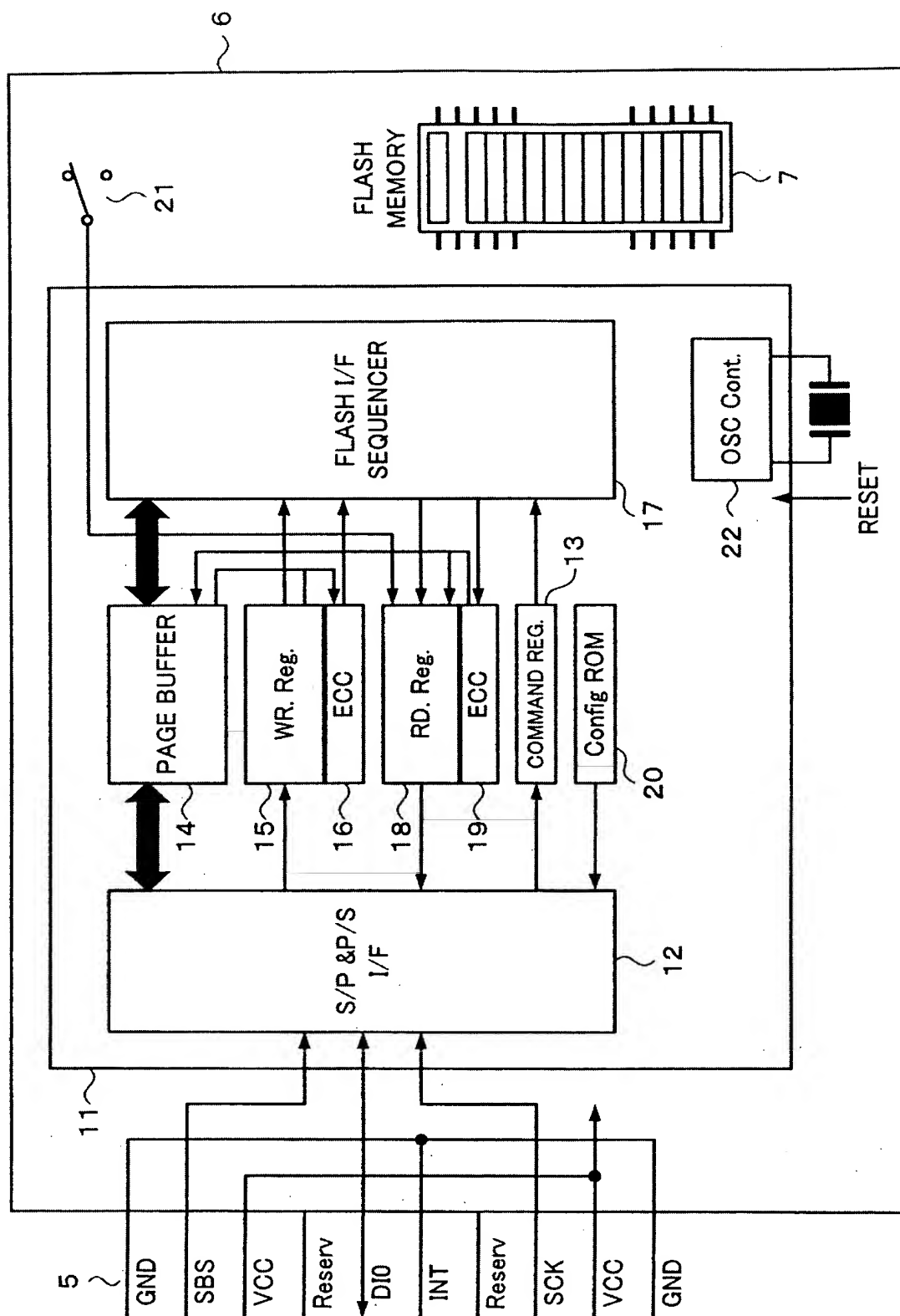


Fig. 3





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Fig. 4

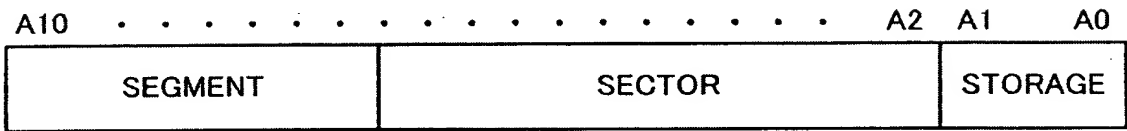
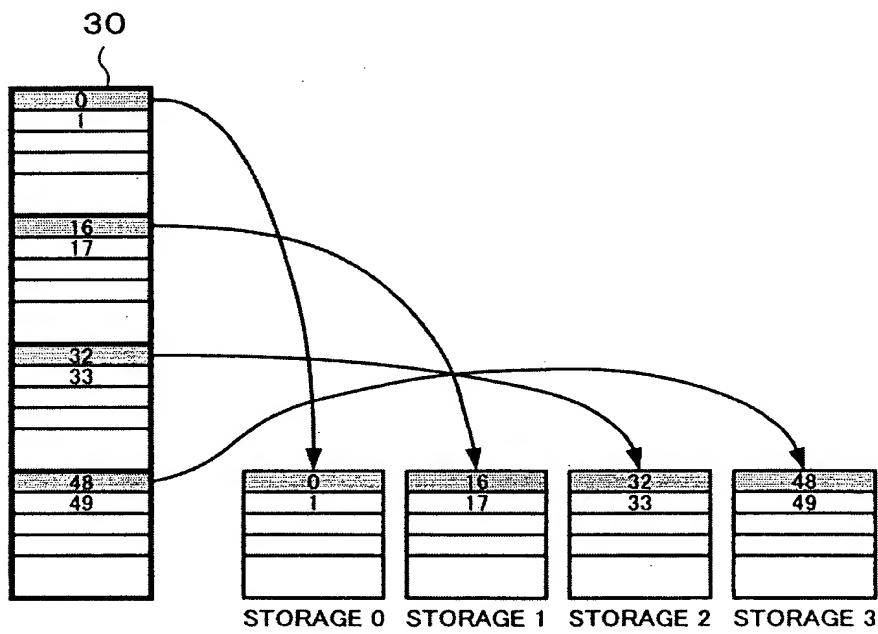
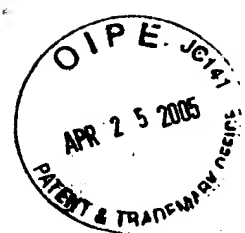


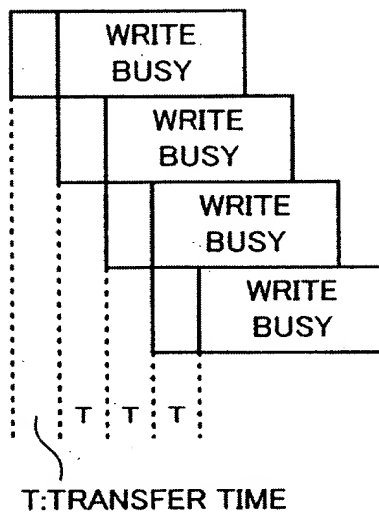
Fig. 5



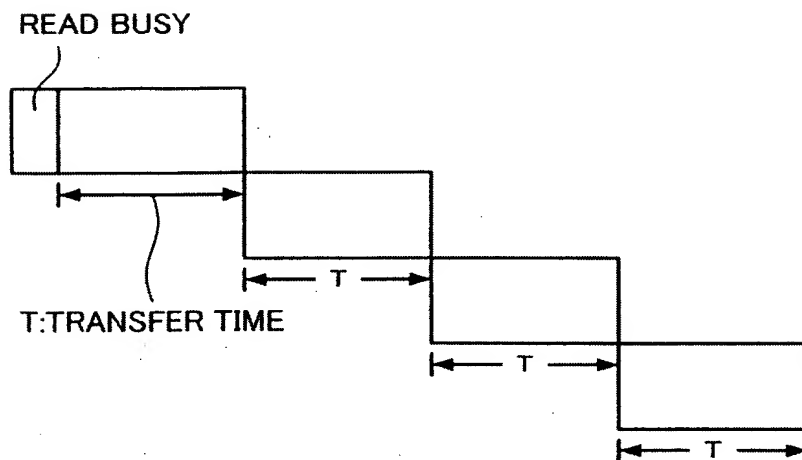


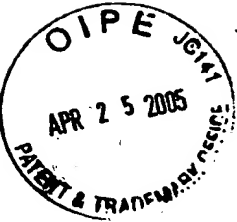
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**Fig. 6**

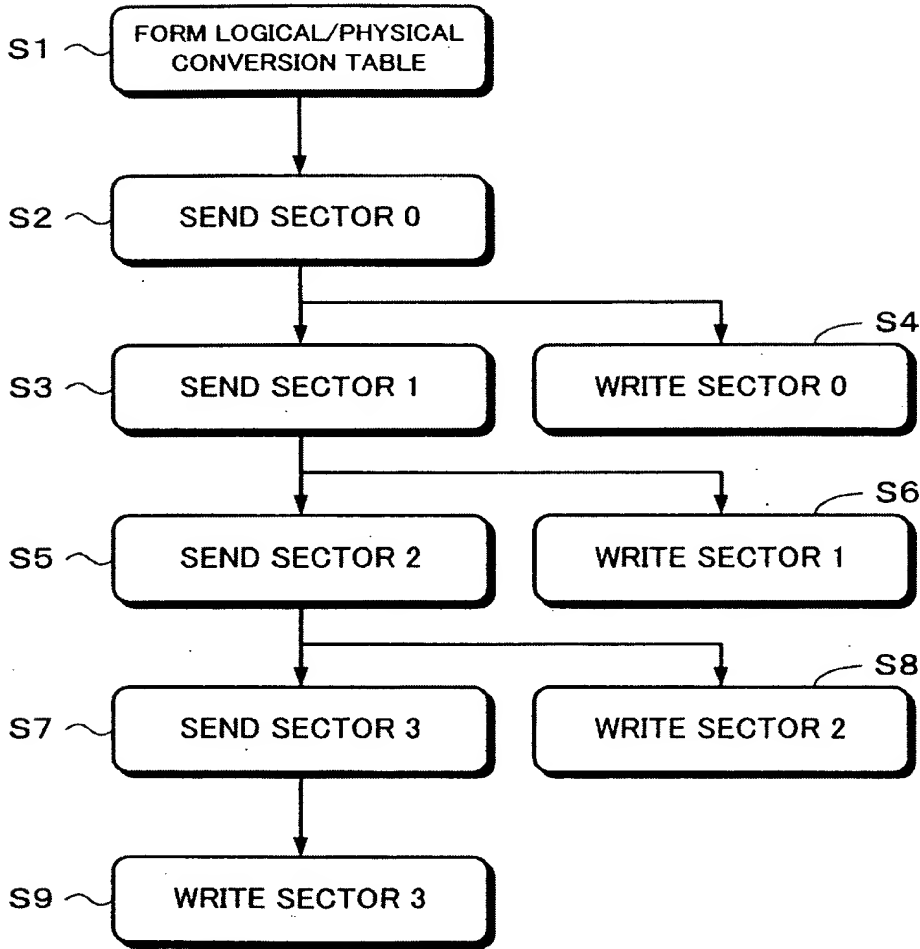


**Fig. 7**





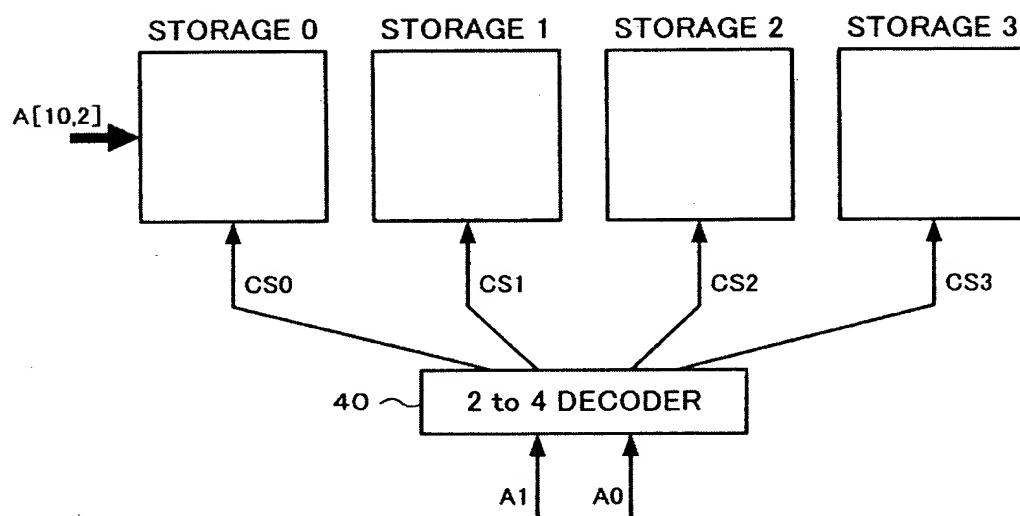
**Fig. 8**

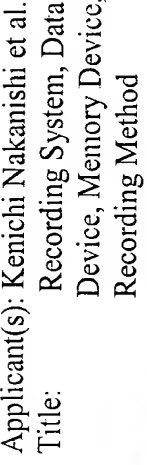




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**Fig. 9**

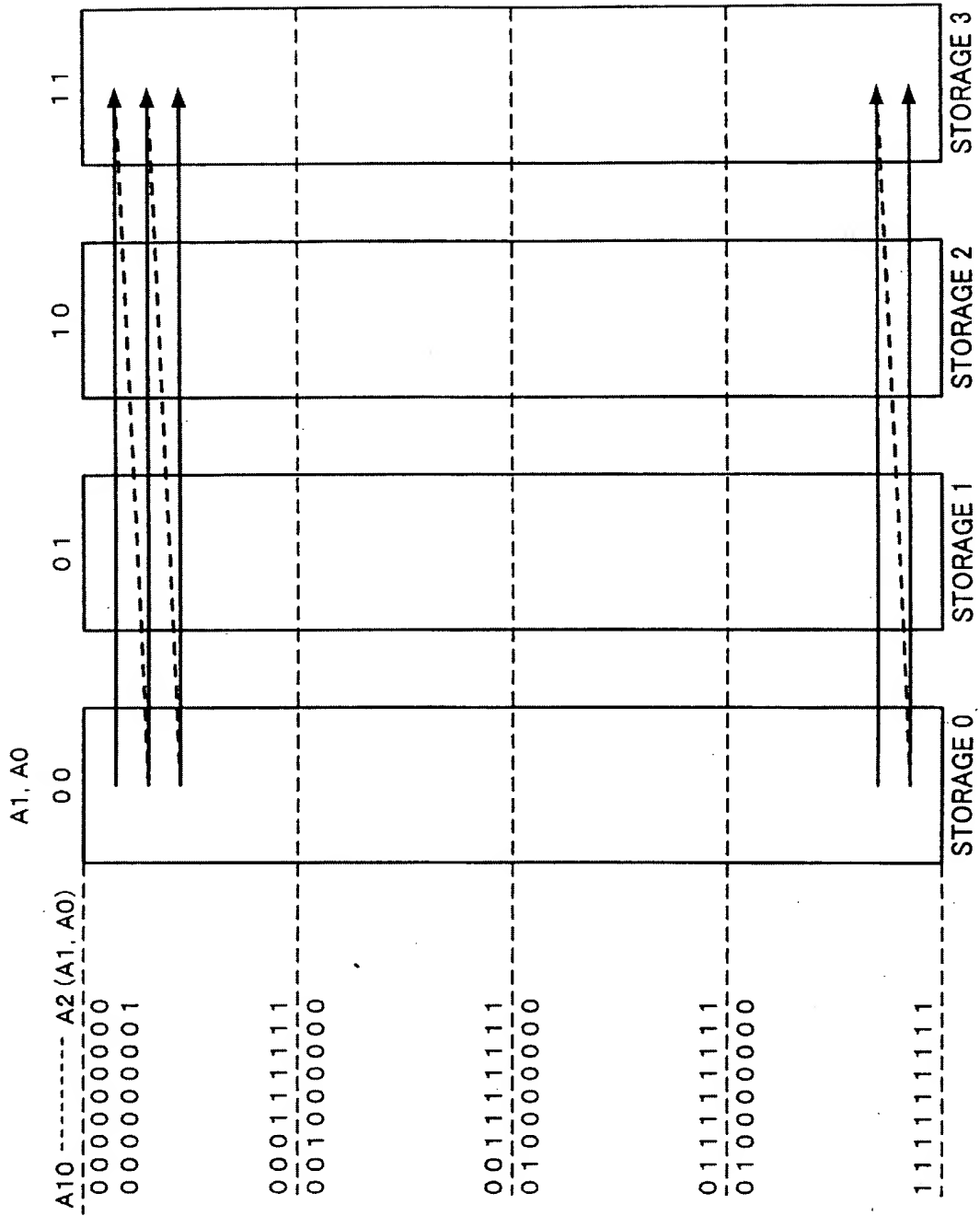


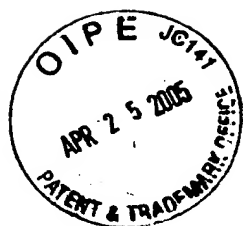


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**Fig. 10**



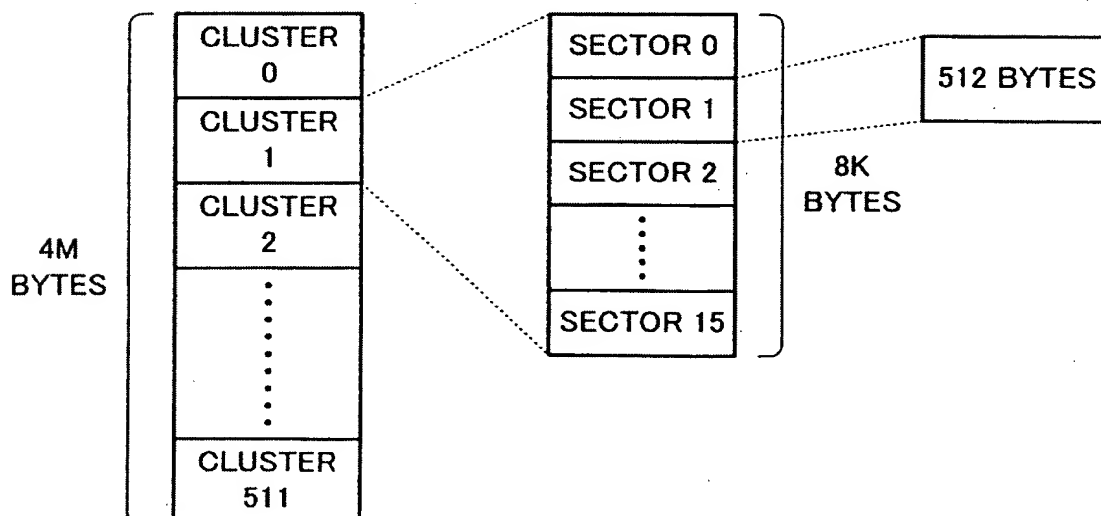


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**Fig. 11**

	STORAGE 0	STORAGE 1	STORAGE 2	STORAGE 3
SEGMENT 0	0x0000	0x0001	0x0002	0x0003
	0x0004	0x0005	0x0006	0x0007
	⋮	⋮	⋮	⋮
	0x01fc	0x01fd	0x01fe	0x01ff
SEGMENT 1	0x0200	0x0201	0x0202	0x0203
	⋮	⋮	⋮	⋮
	0x03fc	0x003fd	0x03fe	0x03ff
SEGMENT 2	0x0400	0x0401	0x0402	0x0403
	⋮	⋮	⋮	⋮
	0x04fc	0x04fd	0x04fe	0x04ff
SEGMENT 3	0x0600	0x0601	0x0602	0x0603
	⋮	⋮	⋮	⋮
	0x07fc	0x07fd	0x07fe	0x07ff

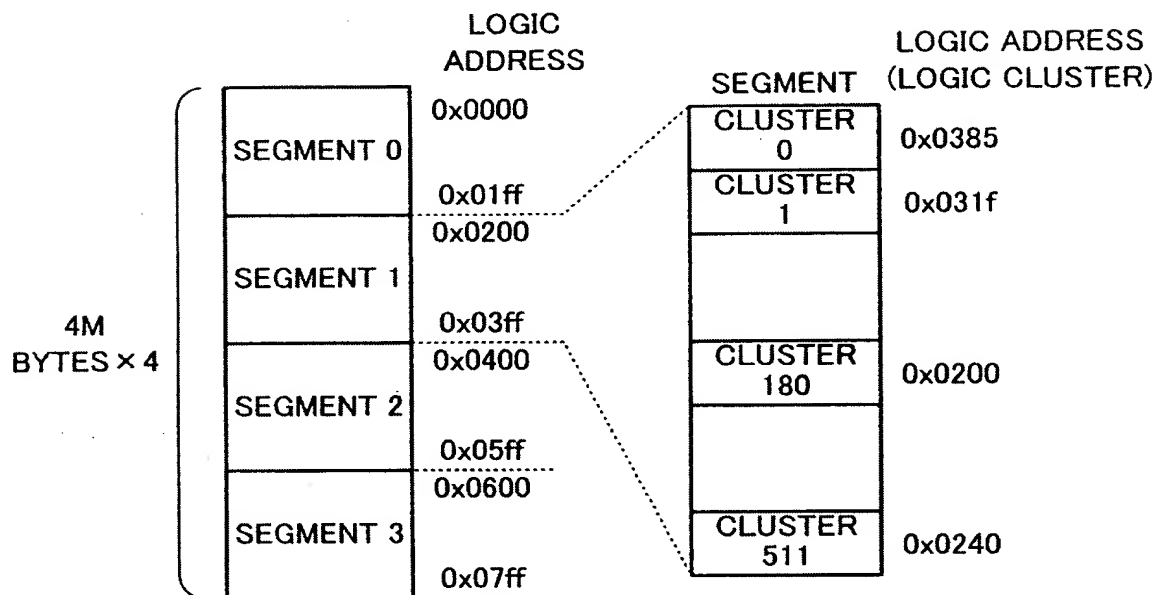
**Fig. 12**





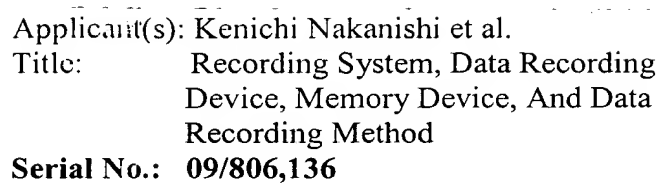
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**Fig. 13A**



**Fig. 13B**

LOGIC ADDRESS	PHYSICAL ADDRESS
0x0200	180
0x0240	511
0x031f	1
0x0385	0



A10	A9	A8	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	A0
STORAGE		SEGMENT					SECTOR											

	WRITE BUSY		WRITE BUSY		WRITE BUSY		WRITE BUSY
--	------------	--	------------	--	------------	--	------------

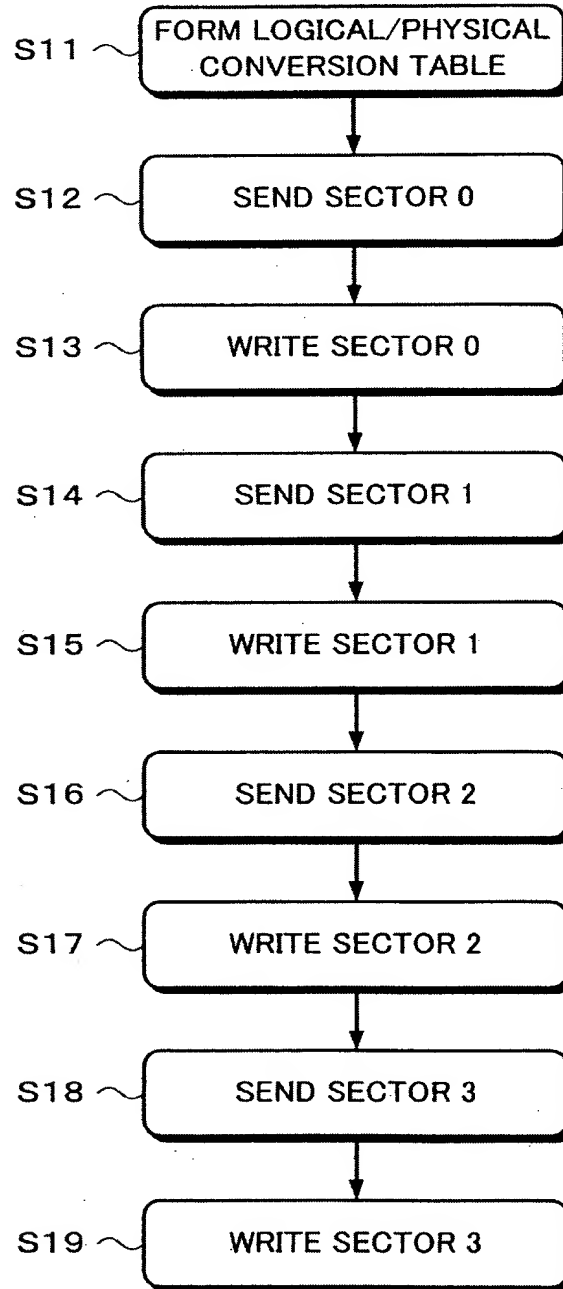
T:TRANSFER TIME

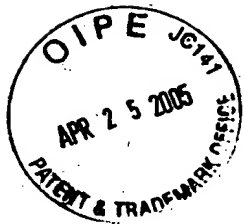
The diagram illustrates a sequence of four data transfers over a bus. Each transfer is represented by a rectangular block labeled 'TRANSFER'. Before each 'TRANSFER' block, there is a period labeled 'READ BUSY'. A bracket below the first 'TRANSFER' block and its preceding 'READ BUSY' period indicates that the total duration of one such cycle is  $T$ .



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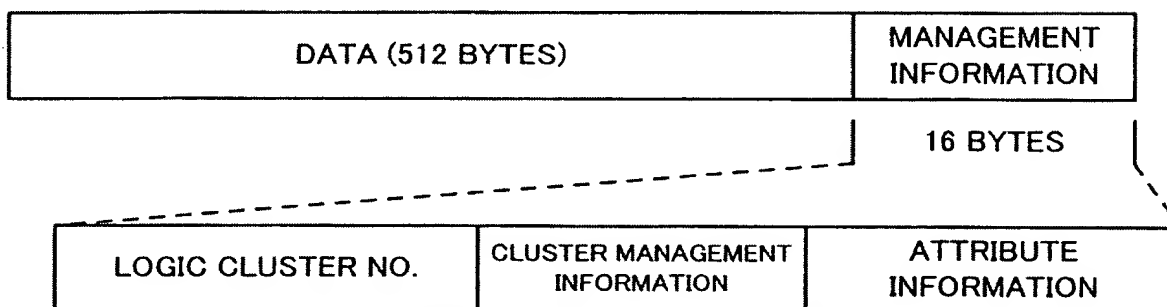
**Fig. 17**



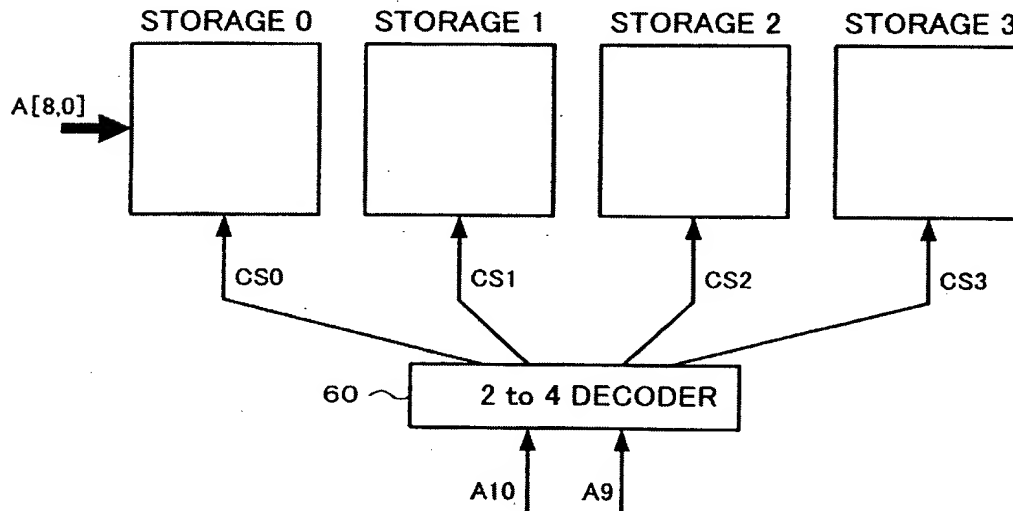


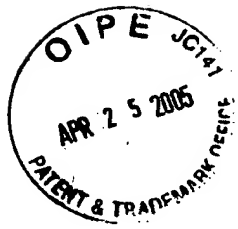
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**Fig. 18**



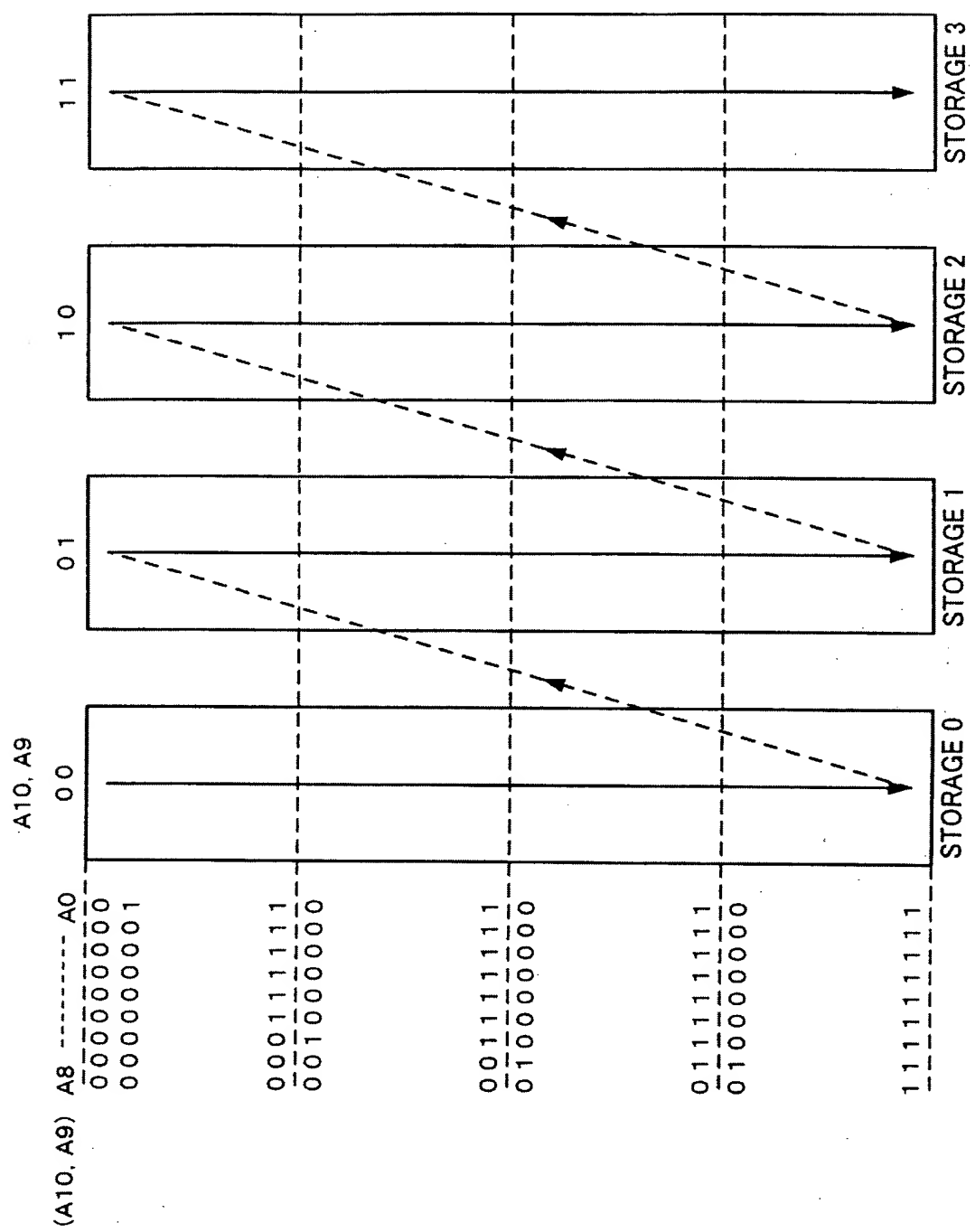
**Fig. 19**

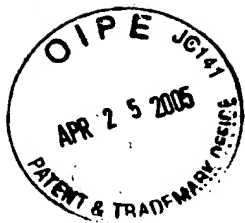




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Fig. 20





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**Fig. 21**

STORAGE 0 SEGMENT 0	STORAGE 1 SEGMENT 1	STORAGE 2 SEGMENT 2	STORAGE 3 SEGMENT 3
0x0000	0x0200	0x0400	0x0600
0x0004	0x0204	0x0404	0x0604
0x0005			
0x0006			
0x0007			
0x01ff	0x03ff	0x05ff	0x07ff